ABSTRACT

A DLL circuit comprises a dummy delay corresponding to an internal clock delay from an external clock, a variable delay addition circuit having a coarse and fine delay circuits adjusting delay amount according to a delay amount adjustment signal, and a phase comparison circuit comparing phases of the internal clock and a delay clock input via the variable delay addition circuit and the dummy delay and outputting the delay amount adjustment signal to the variable delay addition circuit. At the start of burst, a first signal set at a logic "1" during 1 clock cycle of the internal clock is input to the variable delay addition circuit via the dummy delay, and duration time of the logic "1" of the first signal is detected until 1 clock cycle of the internal clock is completed and delay amount of the variable delay addition circuit is initialized by setting one of the coarse delay circuit based on the duration time.